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DOI:
10.1109/TPWRS.2015.2491784

Document Version
Publisher's PDF, also known as Version of record

Citation for published version (Harvard):
Xue, Y, Zhang, X-P & Yang, C 2016, 'Elimination of Commutation Failures of LCC HVDC System with Controllable Capacitors', *IEEE Transactions on Power Systems*, vol. 31, no. 4, TPWRS-00760-2015, pp. 3289. https://doi.org/10.1109/TPWRS.2015.2491784

Elimination of Commutation Failures of LCC HVDC System with Controllable Capacitors

Ying Xue, Xiao-Ping Zhang, *Senior Member, IEEE*, and Conghuan Yang

***Abstract*—This paper presents a novel hybrid converter configuration for conventional Line-Commutated Converter (LCC) HVDC technology aiming to eliminate commutation failures under serious faults. Dynamic series insertion of capacitors during commutation is utilized to increase the effective commutation voltage. The operating principles are presented followed by detailed mathematical analysis for both zero impedance single-phase and three-phase faults in order to select the required capacitor size and its voltage level. The performance of the proposed method is validated by simulation results in Real Time Digital Simulator (RTDS) and the results show that the proposed converter configuration is able to eliminate commutation failures under both fault cases. Consequently partial power transferring capability during single-phase fault and fast fault recovery from three-phase fault can be achieved. Further simulation results show that the harmonic content of inverter AC voltage and current are not significantly increased and the voltage stress of the thyristor valve is comparable to that of the original benchmark system.**

***Index Terms*—Commutation failures, controllable capacitor, HVDC transmission, LCC HVDC, series capacitor insertion.**

I. Introduction

HIGH Voltage Direct Current (HVDC) transmission based on Line-Commutated Converter (LCC) technology has been widely utilized around the world for power transmission since its first application 60 years ago. Although the recent Voltage-Sourced-Converter (VSC) based HVDC technology may be the preferred option for multi-terminal DC grid or wind farm integration, the LCC HVDC still out-performs the VSC in long distance bulk power transmission due to its higher efficiencies. However some well-known problems associated with LCC HVDC still exist today which limits the further application of this technology. The most notable one is commutation failure which can happen under 10%–14% of voltage depression at inverter AC bus [1]. The commutation failure can cause a temporary cessation of power transfer and overheating of the valves. A sudden increase of power transfer between adjacent AC transmission lines can also happen which might affect system transient stability.

Manuscript received May 28, 2015; revised September 02, 2015; accepted October 09, 2015. Date of publication October 26, 2015; date of current version May 02, 2016. Paper no. TPWRS-00760-2015.

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Digital Object Identifier 10.1109/TPWRS.2015.2491784

Commutation failures are frequent dynamic events which are recorded in several practical systems such as the concurrent commutation failures and forced blocking of converter stations in East China Power Grid resulting from single-phase fault at inverter side in 2013 [2]. This accident caused a reduction of 4530 MW power transmitted by HVDC links, which led to a significant reduction of inverter side AC system frequency and an increase of power in the adjacent HVAC lines. Also the generators at rectifier side were tripped and spinning reserves were activated at inverter side to compensate for the loss of active power transfer.

Efforts have been made to reduce the risk of commutation failures and the proposed approaches can be broadly classified into two categories: one is through modification of controllers [3]–[7] and the other is by adding additional capacitive components/power electronic devices [8]–[14].

For the controller modification methods, it has been identified in literature that commutation failures cannot be completely avoided if the fault is electrically close to the inverter [1], [7]. So the objectives of these modifications are either to reduce the probability of commutation failure or to increase the recovery speed of DC system after commutation failure [4]–[6], [15]. The most commonly used method is to advance the firing angle at inverter side immediately after detection of AC voltage disturbance in order to give a larger commutation margin [3]. Another possibility is to reduce the commutated DC current by lowering the current order at rectifier side upon detection of AC voltage disturbance [4]. However the advancement of firing angle will lead to increased reactive power consumption, which will further depress the inverter AC bus voltage particularly for weak AC systems. Also the change of current order at rectifier side might not be fast enough given the normally long distance of the DC link [15].

Among the methods with additions of capacitive components/power electronic devices, Capacitor-Commutated Converters (CCC) [16] was the most popular one which can operate at better power factor and lower probability of commutation failures. However commutation failure still cannot be eliminated and significant increase of voltage stress on thyristors which can be 2 p.u. to 3 p.u. has been identified [8]. Besides CCC, some other researches have been done in the area of active series compensation [11]–[14]. In [11], a small-rated series VSC is added in addition to the fixed series capacitor in CCC. The small rated-VSC is used to actively change its output voltage to compensate the variations of AC voltage while the fixed series capacitor still acts as the main commutation capacitor. The level of AC voltage variation that the series VSC can cope with is limited due to its small rating.

Since the main contributions to commutation failure mitigation are still from the fixed series capacitors so the issues associated with CCC still exist in this topology, and commutation failure elimination is hard to achieve. A similar method using only the series VSC to help mitigate commutation failures is discussed in [14]. The much higher rating of VSC significantly increases the DC voltage harmonic content which can be seen from simulation results in the paper. For commutation failure mitigation, a maximum of 10% AC voltage reduction is simulated so it can be expected that even higher rating of VSC is required for better performance. In [12] a circuit configuration called Controlled Series Capacitor Converter (CSCC) is compared with traditional CCC. CSCC has the series capacitors inserted between filter bus and AC system bus and its capacitor values can be adjusted in a manner similar to that in Thyristor Controlled Series Compensation (TCSC) schemes. However the controllability of capacitors is only used to avoid ferroresonance problem. Considering commutation failure mitigation, it has similar performance with CCC and has the potential risk of increasing valve voltage stress. In [13], the Gate-Commuted Series Capacitor (GCSC) is used at rectifier side for power factor correction. The proposed method can only insert capacitors in one direction and no discussions with regard to commutation failure are presented.

Hence the motivation is strong and potential benefits of further development in eliminating commutation failures are large. It is the aim of this paper to eliminate commutation failure using a novel hybrid converter configuration. The proposed hybrid configuration uses dynamic series capacitor insertion to increase the effective commutation voltage which is the dominant factor for the onset of commutation failures.

This paper is organized as follows. In Section II, the proposed circuit configuration will be described. In Section III, the principles of operation and capacitor voltage balancing issue of the proposed method will be explained. In Section IV, analytical derivations of the commutation period with the inserted capacitors will be presented. Hence guidelines for the selection of capacitor size and its voltage level will then be given based on the derived mathematical relationships. In Section V, the effectiveness of the proposed method will be validated by various simulations in RTDS. Additionally the AC voltage and current harmonic content and thyristor valve voltage stress in the proposed system are compared with the original benchmark system. In Section VI, loss estimation is carried out for the proposed configuration. Both conduction loss and switching loss are estimated. Finally Section VII concludes the paper.

II. Circuit Configuration of Hybrid HVDC Converter

Fig. 1 shows the proposed converter circuit configuration and the connected AC system at inverter side where I_d is the DC current, L_s is the DC smoothing reactor, TY1-TY6 and TD1-TD6 are thyristor valves, CapYa, CapYb, CapYc and CapDa, CapDb, CapDc are the capacitor modules, Z_{inv} and Z_f are equivalent impedances for AC system and filters, respectively. S1Ya-S4Ya are the four Insulated Gate Bipolar Transistor (IGBT) switches for capacitor module CapYa and D1Ya-D4Ya are the associated freewheeling diodes. The whole system is based on the CIGRE HVDC Benchmark model which is a 12-pulse system rated at

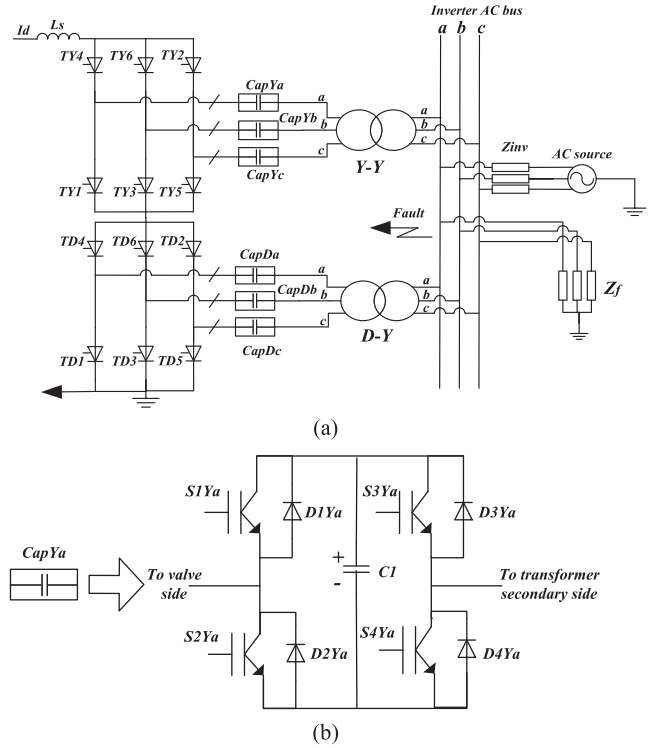

Fig. 1. Proposed inverter topology and connected AC system. (a) System configuration; (b) Capacitor module configuration.

1000 MW, 500 kV and 2 kA with weak AC systems at both ends. Two 6-pulse bridges are connected in series and are connected to the AC system through a YY and a YD transformers enabling partial harmonic cancellations on both AC and DC sides. All the system parameters can be found in [17].

The only additions to the original Benchmark system are the capacitor modules which are connected in series between the secondary side of the converter transformer and the thyristor valves. Each capacitor module can be realized by a single module (as that for 2-level VSC) or by a number of series connected sub-modules to achieve higher insertion voltage. For the sake of the demonstration of the approach, in the following modeling, single capacitor module is assumed. One capacitor module is needed for each phase for a 6-pulse bridge so 6 modules are needed for the 12-pulse HVDC system. It can be seen from Fig. 1 that each capacitor sub-module consists of four IGBT switches with anti-parallel diode across each one of them. The left-hand side of the sub-module is connected to valve side while the right-hand side is connected to the transformer secondary winding.

The reference polarity of the capacitor is shown in Fig. 1. The capacitor will be inserted as a positive voltage when S1 and S4 are switched on and S2 and S3 are switched off. The capacitor will be inserted as a negative voltage when S2 and S3 are switched on and S1 and S4 are switched off. The capacitor can be bypassed when S1 and S3 are on or S2 and S4 are on at the same time. To enable comparisons with the original Benchmark system the converter control system at both ends are kept the same as the benchmark model except that the rectifier firing angle is temporarily limited at high DC current which will be explained in later sections.

III. Insertion Strategies

A. Commutation Failure

Theoretical analysis of commutation failure is perhaps best presented in [1], which concludes that the inverter AC voltage magnitude reduction is the most dominant factor for commutation failure under both single-phase and three-phase fault. Voltage phase angle shift is also the reason for the onset of commutation failure under single-phase fault but to a lesser extent than magnitude reduction. Another important conclusion is that other than modifying the extinction angle setting, other modifications to the DC control system will not significantly affect the onset of initial commutation failure. It is due to fact that control system will not be able to react if a serious fault happens at the start or during the process of commutation. So the goal of control system modification can be mostly useful to prevent successive commutation failures or to increase the recovery speed of the system. However if the aim is to eliminate commutation failures rather than reduce its probability, the most direct way is to increase the effective commutation voltage. The most commonly used method is to add Static Var Compensator (SVC) or Static Compensator (STATCOM) at the inverter AC side for dynamic reactive power support to regulate AC voltage. The effectiveness of SVC in mitigating commutation failure was limited given its relatively slow response time. The rapid control of STATCOM will certainly give some improvements but will not be very useful under low impedance grounding fault at inverter AC bus. So in this paper dynamic series insertion of capacitors to increase the effective commutation voltage is adopted to eliminate the commutation failures under zero impedance single-phase and three-phase faults. The usefulness of the method then largely depends on the insertion strategy, selection of capacitor voltage level and capacitance value which are described in following sections.

B. Operating Principles

The insertion strategy is called 'push' & 'pull' method where two capacitor modules (or the two sets of series connected capacitor sub-modules) in both outgoing phase and incoming phase are inserted at the same time. The principles of operation can be illustrated with reference to Fig. 2 where the commutation from TY2 to TY4 is considered. In Fig. 2, i_2, i_3 and $i_4$are instantaneous currents through TY2, TY3 and TY4, respectively and L_c is the transformer leakage inductance. Only the upper 6-pulse bridge is considered for explanation but the principle is the same for lower 6-pulse bridge. Before the start of commutation, TY2 and TY3 will be conducting with all three capacitors bypassed. The capacitor voltages are assumed to be positively charged to the polarity as shown in Fig. 1. At the instant of firing TY4, CapYc will be inserted as a positive voltage and CapYa will be inserted as a negative voltage until commutation is complete. Observing the loop containing TY4 and TY2, it can be seen that the resulting commutation voltage between phase C and phase A is increased. The amount of increase is equal to the sum of two capacitor voltages. During extreme fault conditions when the inverter AC commutation voltage is significantly reduced, the commutation voltage will

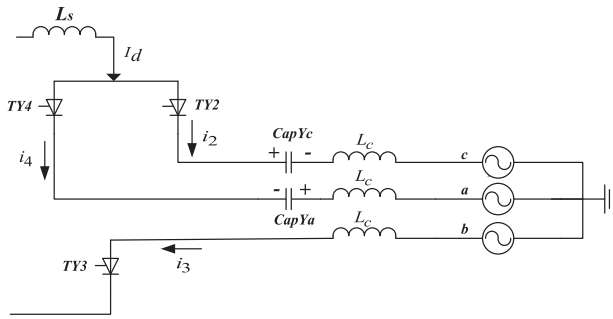

Fig. 2. 'Push' & 'Pull' method of capacitor insertion.

primarily come from the two inserted capacitors. This additional commutation voltage can prevent commutation failures from happening if the capacitor size and its charging level are appropriately chosen. At the end of commutation, the capacitor voltage in phase C increases and capacitor voltage in phase A decreases due to the directions of current flows through them.

It is important to point out that during the next commutation period, which is from TY3 to TY5, CapYc will also be inserted as a positive voltage to help the commutation process. However since this time the current in phase C will be flowing in the opposite direction so CapYc will discharge and its voltage level will decrease at the end of commutation. The level of capacitor voltage change during two successive commutation processes is determined by the value of capacitor. In this way each capacitor voltage is partially balanced and additional charging/discharging actions outside commutation period are reduced in order to keep a constant capacitor voltage level.

C. Capacitor Voltage Balancing

As discussed before the capacitor voltages are partially balanced due to the conduction sequence of thyristors. Therefore only limited insertion times are required to keep capacitor voltage around the reference value. The main firing logics for capacitor voltage balancing can be illustrated by considering the capacitor module CapYa as shown in Fig. 1. Since CapYa is connected to TY4 and TY1 so it can only be charged or discharged when TY4 or TY1 is fully conducting. In order to reduce the number of switching actions, the period when TY4 is conducting is chosen for the charging of CapYa. A PI controller is used to minimize the voltage difference between reference capacitor voltage V_{c_ref} and measured capacitor voltage $VYYa_{meas}$. The output of the controller is the firing angle α_{YYa} at which CapYa will be inserted as a positive voltage. The phase reference for the actual insertion time is θ_{YYa}. It is obtained by shifting the PLL phase output for inverter AC bus voltage. Similarly, the phase reference for CapDa which is connected with YD transformer is obtained by adding an additional 30° of phase shift to θ_{YYa}. Similar methods are used to get the phase references for other capacitor modules. In this specific case CapYa will be inserted as a positive voltage for a short time duration before the firing of TY6 and it is bypassed when the commutation from TY4 to TY6 is complete. Fig. 3 shows the block diagram representation of how the firing logics for CapYa voltage balancing are implemented. The firing

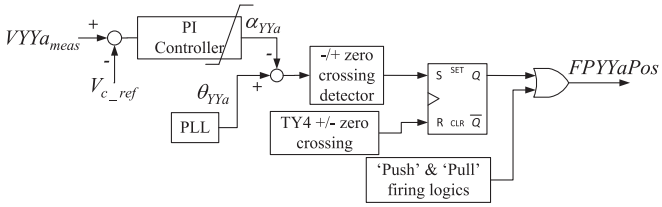

Fig. 3. Firing logics for CapYa voltage balancing.

logics for all the other capacitor modules will have the similar structure.

IV. Theoretical Analysis and Parameter Selection

The success of the proposed method depends on the selection of parameters which are capacitor value and its voltage level. The size of capacitor is mainly determined by its percentage of voltage change after each commutation, and a too small capacitor size resulting in significant voltage changes during commutation is not desirable. The nominal voltage level of the capacitor is determined so that commutation can still be successful under extreme fault conditions. In order to have a better insight into the problem, analytical formulation regarding the commutation process with the proposed insertion strategy is utilized to help the selection of both parameters.

A. Commutation With Capacitor Insertion

Without losing generality the commutation period from TY1 to TY3 as shown in Fig. 4 is considered in this section. The referred instantaneous line-to-neutral voltages are

$$\begin{aligned} e_a &= E_m \cos(\omega t + 60^\circ) \\ e_b &= E_m \cos(\omega t - 60^\circ) \\ e_c &= E_m \cos(\omega t - 180^\circ) \end{aligned} \tag{1}$$

where E_m is the magnitude of phase voltage and ω is the AC system angular frequency. The transformer turns ratio for both YY and YD transformers are 254:211.42 (primary: secondary). In Fig. 4, C is the capacitor value, v_n is the instantaneous voltage for the capacitor inserted in negative direction and v_p is the instantaneous voltage for the capacitor inserted in positive direction, i_1 and i_3 are instantaneous currents flowing through TY1 and TY3, respectively. The polarity of the voltages and directions of current flow are as shown in Fig. 4. It is assumed that the DC current I_d will be constant, the capacitor voltages are pre-charged to V_0 in the commutation circuit loop. For the circuit loop containing TY1 and TY3, the dynamic equations can be written as follows:

$$i_1 + i_3 = I_d \tag{2}$$

$$i_1 = C\frac{dv_n}{dt} \tag{3}$$

$$i_3 = -C\frac{dv_p}{dt} \tag{4}$$

$$e_b - L_c\frac{di_3}{dt} + v_p = e_a - L_c\frac{di_1}{dt} - v_n \tag{5}$$

With the initial conditions

$$v_p(t)|_{t=\frac{\alpha}{\omega}} = V_o \tag{6}$$

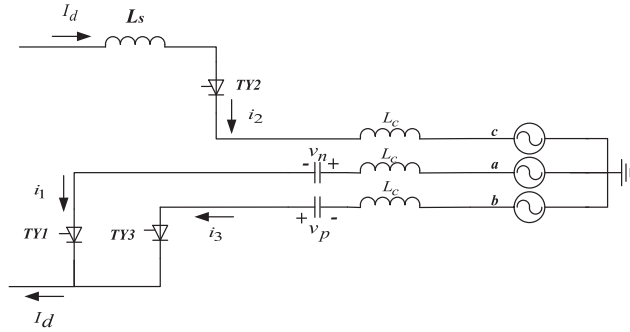

Fig. 4. Commutation from TY1 to TY3.

$$\frac{dv_p(t)}{dt}|_{t=\frac{\alpha}{\omega}} = -\frac{1}{C}i_3|_{t=\frac{\alpha}{\omega}} = 0 \tag{7}$$

where α is the firing angle and ω is the rated frequency of the AC system. Solve the sets of differential equations in (2)–(5) gives the following result:

$$v_p = C_1 cos\omega_n t + C_2 sin\omega_n t + Bsin\omega t + D \tag{8}$$

where

$$C_1 = aV_0 - Basin\alpha - \frac{bI_d}{2\omega_n C} + \frac{Bb\omega}{\omega_n}cos\alpha \tag{9}$$

$$C_2 = bV_0 - Bbsin\alpha + \frac{aI_d}{2\omega_n C} - \frac{Ba\omega}{\omega_n}cos\alpha \tag{10}$$

$$a = \cos\frac{\omega_n}{\omega}\alpha \tag{11}$$

$$b = \sin\frac{\omega_n}{\omega}\alpha \tag{12}$$

$$\omega_n = \frac{1}{\sqrt{L_c C}} \tag{13}$$

$$B = \frac{-\sqrt{3}E_m}{2L_c C} \times \frac{1}{\omega_n^2 - \omega^2} \tag{14}$$

$$D = -\frac{I_d}{2C}t + \frac{I_d\alpha}{2\omega C} \tag{15}$$

The current i_3 can then be found by substituting (8) into (4)

$$i_3 = -C\left(-C_1\omega_n \sin\omega_n t + C_2\omega_n \cos\omega_n t + B\omega\cos\omega t - \frac{I_d}{2C}\right) \tag{16}$$

B. Capacitor Voltage Level

As discussed earlier, the capacitor voltage level will be selected so that commutation can still be completed under extreme fault conditions such as zero impedance single-phase grounding fault or three phase grounding fault. In the following analysis, both the zero impedance three-phase and single-phase faults will be considered, respectively, for the selection of capacitor voltage level.

1) Three-Phase Fault: In the case of zero impedance three-phase fault at inverter AC bus E_m will be zero. Hence there will be no commutation voltage from AC side and the commutation voltage is completely coming from the inserted capacitors. This condition sets the basic minimum capacitor voltage required for successful commutation under three-phase fault.

In addition to the zero AC commutation voltage, the DC current which needs to be commutated from one valve to another

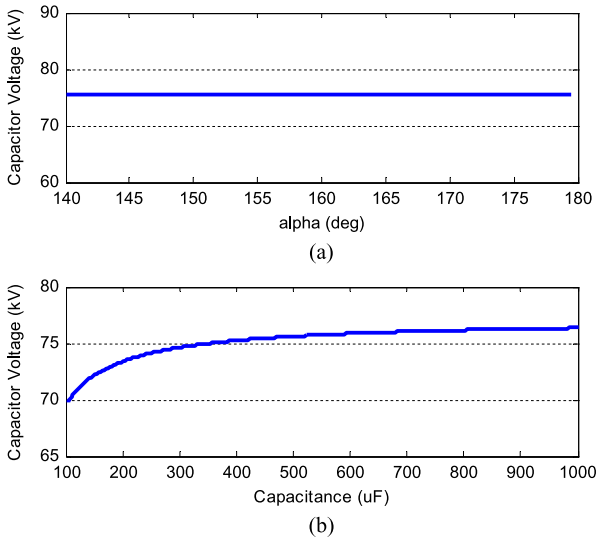

Fig. 5. Variation of required capacitor voltage level for three-phase fault. (a) With firing angle from 140° to 180°; (b) With Capacitor value from 100 μF to 1000 μF.

can be very large during three-phase fault. For the benchmark system with a rated 2 kA DC current, the peak DC current $I_{d\max}$ of around 4 kA is chosen as the maximum peak DC current during fault cases.

Another aspect which needs to be considered is the maximum allowable overlap angle$\mu_{\max}$. Ideally the commutation has to be completed before the next valve fires. For example in the case of commutation from TY1 to TY3, it has to be completed before TY4 fires, which is 60° later after the firing of TY3. In this paper considering the recovery time of thyristors to regain forward blocking capability, a commutation safe margin of 20° is chosen to ensure successful commutation during fault, and hence $\mu_{\max}$ is chosen to be 40°.

Now the necessary condition for successful commutation under zero impedance three-phase fault can be written as

$$i_3|_{t=\alpha+\mu_{\max},I_d=I_{d\max}} \geq I_{d\max} \tag{17}$$

where

$$E_m = 0\ \text{kV} \tag{18}$$
$$\mu_{\max} = 40^\circ \tag{19}$$
$$I_{d\max} = 4\ \text{kA} \tag{20}$$

In order to solve (17) for the minimum capacitor voltage level $V_{0\min}$, the capacitor value C will be preliminary set to 500 μF and it will be shown later that capacitor value will not significantly affect $V_{0\min}$ once (18)–(20) are defined.

Fig. 5 shows the variation of $V_{0\min}$ with different firing angles and capacitor values by solving (17). It can be seen that in the absence of natural commutation voltage, the value of firing angle has no impact on the value of $V_{0\min}$ which has a constant value of about 76 kV from the selected criteria. It can also be seen from Fig. 5(b) that $V_{0\min}$ is relatively insensitive to the capacitor value.

2) Single-Phase Fault: In this case zero impedance phase A to ground fault will be considered thus only phase B voltage e_b will produce the commutation voltage. In addition, the phase shift on e_b due to phase A fault has to be considered. If the remaining two phases are kept balanced at the time of fault, then the phase shift introduced on e_b will be 30°. By setting $e_a = 0$ in (5) and considering the 30° phase shift in e_b, re-solve equations (2)–(5) with initial conditions (6)–(7), valve 3 current under single-phase fault can be got as

$$i_3' = -C\left[-C_1'\omega_n \sin\omega_n t + C_2'\omega_n \cos\omega_n t - B'\omega\sin(\omega t - 30^\circ) - \frac{I_d}{2C}\right] \tag{21}$$

where

$$C_1' = aV_0 - Ba\cos(\alpha - 30^\circ) - \frac{bI_d}{2\omega_n C} - \frac{Bb\omega}{\omega_n}\sin(\alpha - 30^\circ) \tag{22}$$

$$C_2' = bV_0 - Bb\cos(\alpha - 30^\circ) + \frac{aI_d}{2\omega_n C} + \frac{Ba\omega}{\omega_n}\sin(\alpha - 30^\circ) \tag{23}$$

$$B' = \frac{-E_m}{2L_c C} \times \frac{1}{\omega_n^2 - \omega^2} \tag{24}$$

Now the necessary condition for successful commutation under zero impedance single-phase fault is

$$i_3'|_{t=\frac{\alpha+\mu_{\max}}{\omega},I_d=I_{d\max}} \geq I_{d\max} \tag{25}$$

Together with 500 μF of capacitor value and (19)–(20), the capacitor voltage requirement with different firing angles for single-phase fault can be obtained by solving (25). Fig. 6(a) shows the variation of $V_{0\min}$ against firing angle from 140°–180°. By comparing with Fig. 5(a) it can be seen that this time as α increases the required capacitor voltage level also increases due to the negative commutation voltage produced by e_b. This point can be made clearer with reference to Fig. 7 which shows the commutation from TY1 to TY3 fails due to phase A to ground fault. By observing Fig. 7 it can be found that at the start of commutation when TY3 is fired, the total commutation voltage e_{ba} is negative and as commutation continues this negative commutation voltage becomes larger which results in significant increase of the required capacitor voltage for successful commutation. Further results in Fig. 6(b) show that it is the inverter firing angle that mainly affects the required capacitor voltage level rather than the capacitor value in the case of single-phase fault.

Hence the dynamics of inverter firing angle during fault conditions should also be considered for the voltage level selection. Given that the normal time constant for inverter extinction angle controller is relatively large compared with the fast transients during commutation failures, the inverter firing angle will not significantly vary during the first few cycles after a fault. Considering this together with the results shown in Fig. 5 and Fig. 6, the capacitor voltage level required for successful commutation under both single-phase and three-phase grounding faults is chosen to be 140 kV for our simulation studies.

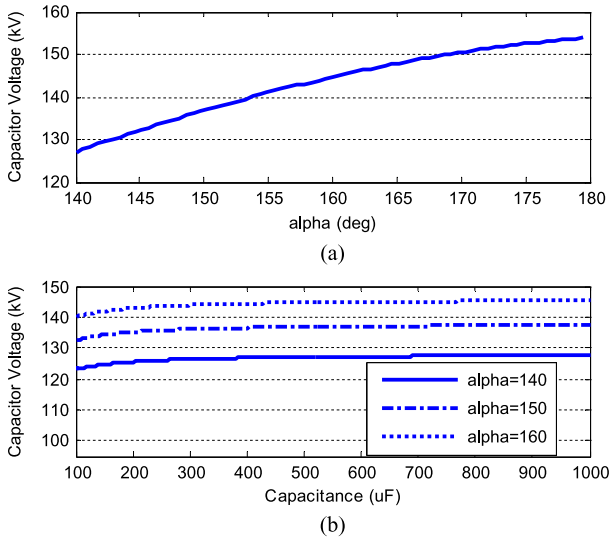

Fig. 6. Variation of required capacitor voltage level for single-phase fault. (a) With firing angle from 140° to 180°; (b) With Capacitor value from 100 μF to 1000 μF.

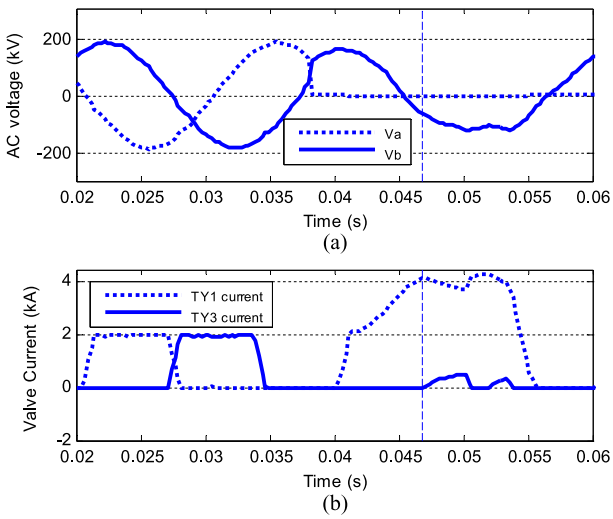

Fig. 7. Commutation failure under Phase A to ground fault. (a) Voltage; (b) Valve currents.

C. Capacitor Value

After the capacitor voltage level is determined, the capacitor value will be selected considering the level of voltage change after each commutation. It should be noted that generally the change of voltages for v_p and v_n are not the same so they need to be calculated separately. The percentages of voltage change for v_p and v_n are given as

$$P_p = \frac{V_0 - v_p(t)|_{t=\frac{(\alpha+\mu)}{\omega}}}{V_0} \times 100\% \tag{26}$$

$$P_n = \frac{v_n(t)|_{t=\frac{(\alpha+\mu)}{\omega}} - V_0}{V_0} \times 100\% \tag{27}$$

where v_n can be calculated by substituting (3) and (4) into (2) and then take definite integral with respect to t which gives

$$v_n(t) = v_p(t) + \frac{I_d}{C}(t - \alpha/\omega) \tag{28}$$

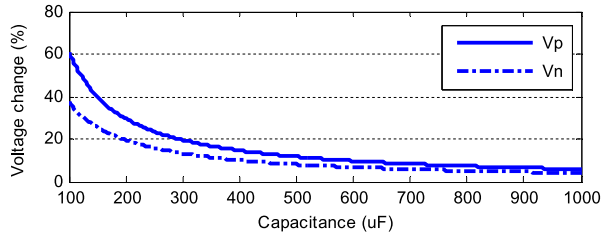

Fig. 8. Percentage of voltage change of capacitor under three-phase fault.

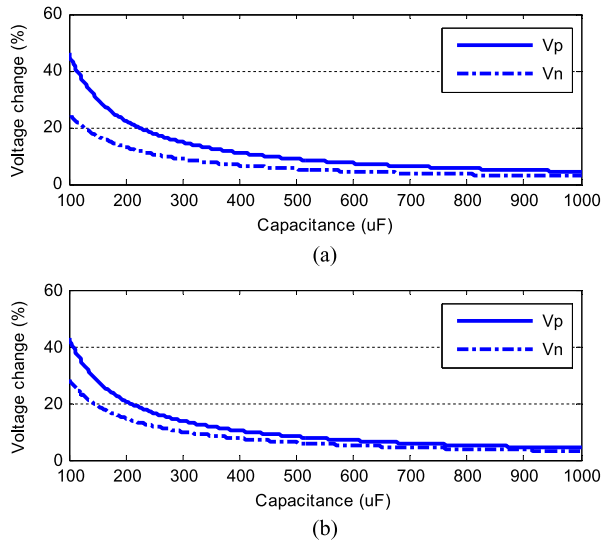

Fig. 9. Percentage of voltage change under single-phase fault. (a) $\alpha = 140°$; (b) $\alpha = 150°$.

It is expected that the greatest change of voltage will happen during fault conditions thus the maximum voltage change during both faults will be used as the selection criteria.

1) Three-Phase Fault: Fig. 8 shows how the percentage of voltage reduction is related to the capacitor values. The results of the figure are got based on (18)–(20). It can be seen that for all the capacitor values in the considered range the increase of v_n at outgoing phase is always smaller than the decrease of v_p at incoming phase. Also in order to get acceptably small voltage reduction after each commutation the capacitor value should be reasonably large.

2) Single-Phase Fault: Fig. 9 shows the results for single-phase fault. Compared with Fig. 8 the results are quite similar and it can be found from Fig. 9(a) and Fig. 9(b) that change of firing angle does not have a significant impact on the voltage variations.

Based on the results shown in Fig. 8 and Fig. 9, if a maximum 10% voltage variation is chosen then the capacitor value can be selected to be 585 μF.

V. Simulation Results

This section presents simulation results based on the CIGRE HVDC benchmark model using the proposed method and calculated component parameters to validate the theoretical analysis. Comparisons with CCC-HVDC are also carried out to verify the results. The whole system is set up in RTDS and for the accuracy of results, the whole DC system including the added capacitor

modules are modelled inside the RSCAD 'VSC small time-step box' with a small simulation time-step of 3.6 μs.

The usual method in studies relating to commutation failure is to apply faults at various electrical distances to produce different levels of voltage drop at inverter AC side and then plot the probability of commutation failures using the point-on-wave way of fault application. However for the proposed method, since commutation failures can be eliminated, only the worst cases of faults which are zero impedance single-phase and three-phase faults are shown for the purpose of illustration. Since line-to-line and double-line-to-ground faults are less severe and are not the main cause of commutation failures in practical systems, they are excluded in simulation study. Also in simulation studies, the rectifier side firing angle is temporarily limited to 60 degrees once the rectifier side DC current is higher than 2.5 kA. This is added so that rectifier current controller does not increase its firing angle too much to result in a low DC voltage and zero DC current during a fault. Because of the elimination of commutation failures, this modification results in a reasonable DC current during a fault and facilitates a faster system recovery.

A. Fault Dynamics

Fig. 10 shows the system responses with a zero impedance phase C to ground fault of 50 ms at the inverter AC bus. The fault is triggered at the same time when one of the commutation starts. Responses from the original CIGRE benchmark are included as comparison. It can be seen from the figure that although the phase voltage drops to zero during the fault, the DC voltage is kept positive in the proposed system. Fig. 10(c) shows clearly that there is no commutation failure in the proposed system while in Fig. (d), it can be seen that commutation failure is happening due to the fault. Therefore the proposed system is able to transfer about 40% of the rated power during single-phase to ground fault. The benchmark system is not able to transmit power to the inverter AC system due to the DC short circuit during commutation failures. Fig. 10(e) shows that the proposed system recovers to 90% of the rated power in about 80 ms after the fault is cleared which is faster than that in the benchmark system. Fig. 10(f) shows that the capacitor voltages are well controlled throughout the fault period.

Fig. 11 shows the system response with a zero impedance three-phase to ground fault of 100 ms. Responses from both the proposed system and the benchmark system are shown for comparison. It can be seen from Fig. 11(c) that in complete absence of natural commutation voltage from AC side, the commutations are still successful. On the other hand for the benchmark system, commutation failures are obvious which can be seen from Fig. 11(d). The slightly higher peak current in Fig. 11(c) is due to the limitation of rectifier firing angle during the fault. Fig. 11(e) shows that both systems are able to recover to 90% of its rated power in about 100 ms but the initial recovery speed of the proposed system is faster due to the elimination of commutation failures. It can also be observed in Fig. 11(f) that capacitor voltages are well controlled.

In order to verify the results, responses of the proposed system under zero impedance single-phase and three-phase faults are compared to those from CCC-HVDC. The CCC-HVDC system is set up by modifying the original CIGRE

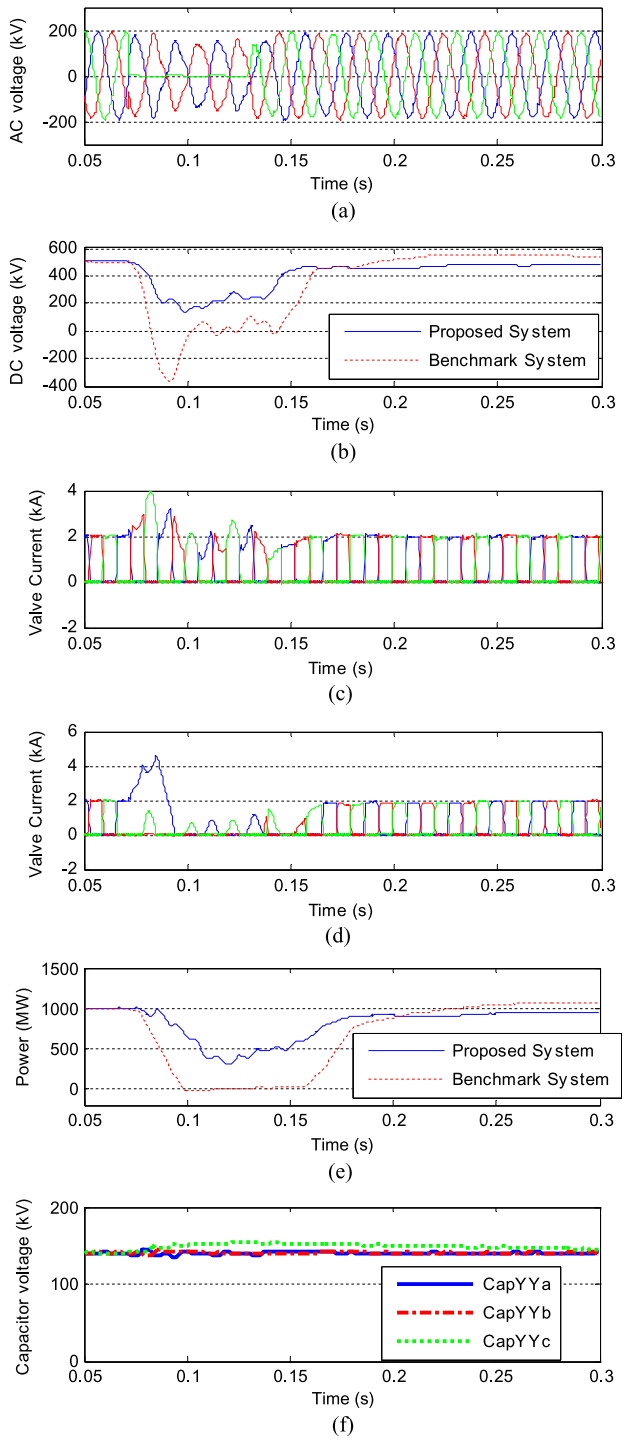

Fig. 10. System response with 50 ms zero impedance single-phase to ground fault at inverter AC bus. (a) AC voltages; (b) Inverter DC voltages; (c) Valve currents (TY2, TY4 and TY6) of the proposed system; (d) Valve currents (TY2, TY4 and TY6) of the CIGRE HVDC benchmark system; (e) Active Power; (f) Capacitor voltages (CapYYa, CapYYb, CapYYc).

HVDC benchmark model. The values for series capacitors are 92.6 μF and the filter banks are modified to provide 15% of the reactive power. At normal operating point the rated apparent extinction angle γ_{app} is controlled to be 2°, which corresponds to an actual extinction angle of about 27°. The transformer turns ratio is also modified to match nominal working condition.

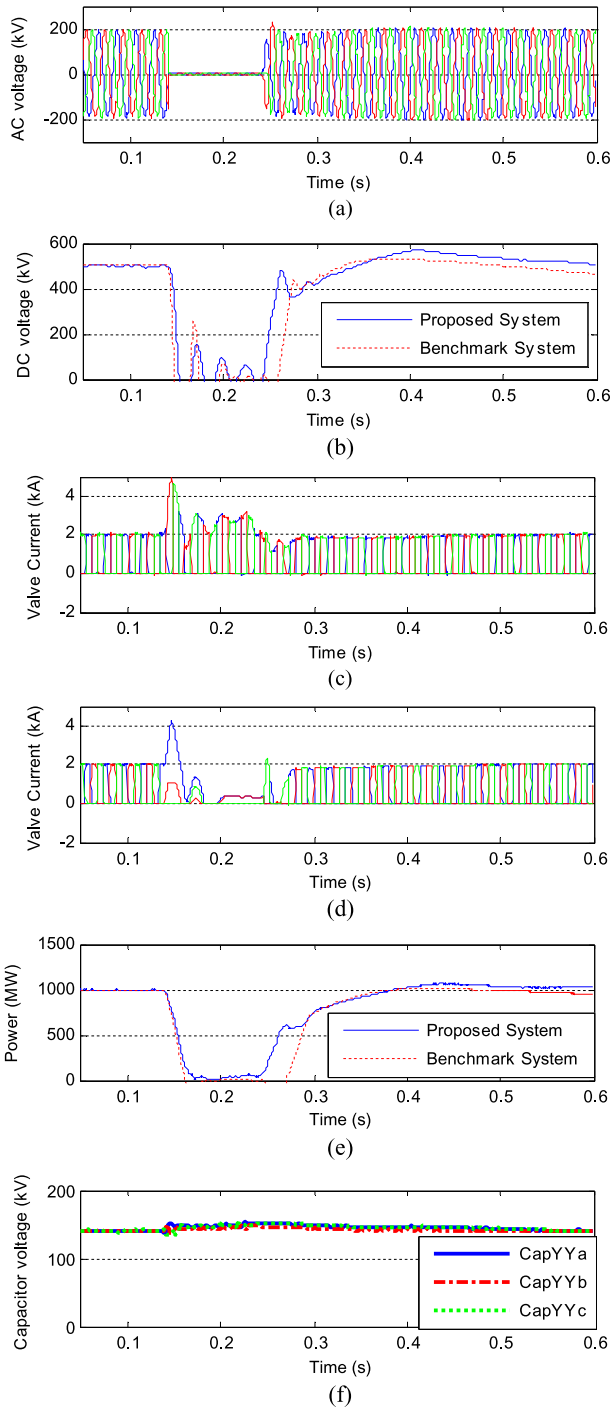

Fig. 11. System response with 100 ms zero impedance three-phase to ground fault at inverter AC bus. (a) AC voltages; (b) Inverter DC voltages; (c) Valve currents (TY2, TY4 and TY6) of the proposed system; (d) Valve currents (TY2, TY4 and TY6) of the CIGRE HVDC benchmark system; (e) Active Power; (f) Capacitor voltages (CapYYa, CapYYb, CapYYc).

Simulation results for single-phase fault are shown in Fig. 12. It can be seen from Fig. 12(d) that although there is improvement in commutation after the initiation of fault for CCC-HVDC, commutation failure still happens. Hence the recovery speed of CCC-HVDC is slower than that for the proposed system.

Fig. 13 shows the simulations results for three-phase fault. It can be seen from Fig. 13(d) that the first few commutations

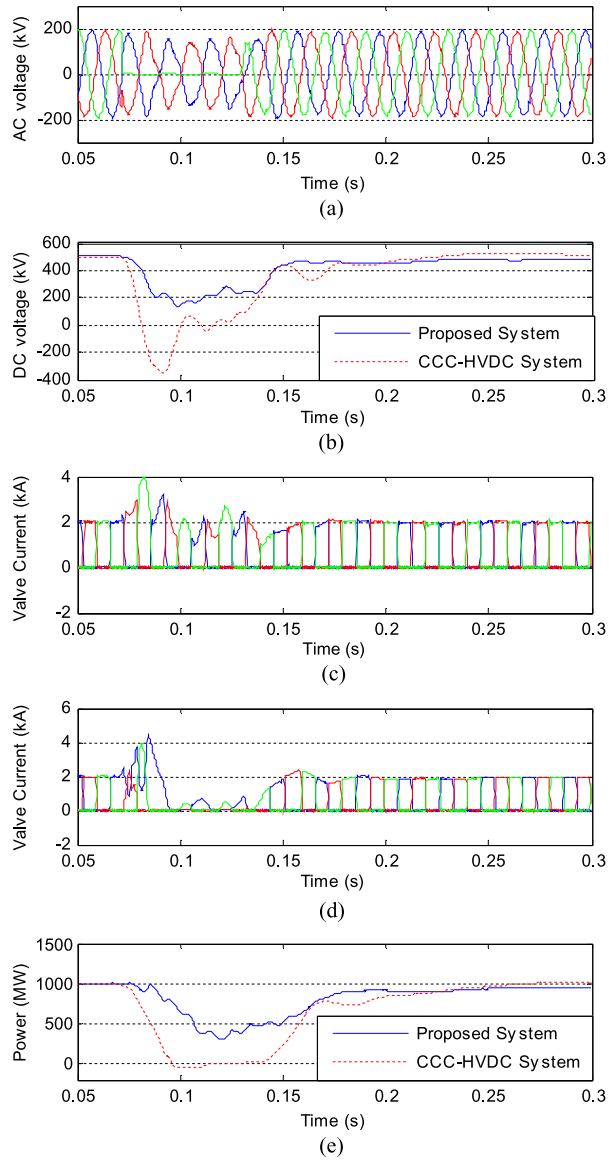

Fig. 12. System response with 50 ms zero impedance single-phase to ground fault at inverter AC bus. (a) AC voltages; (b) Inverter DC voltages; (c) Valve currents (TY2, TY4 and TY6) of the proposed system; (d) Valve currents (TY2, TY4 and TY6) of CCC-HVDC; (e) Active Power.

after the fault are successful due to extra commutation margin and commutation voltage from the series capacitors. However commutation failure still happens later on during the fault when capacitor voltages drop.

B. Capacitor Voltage Dynamics

Detailed simulation waveforms are presented in Fig. 14 to demonstrate the effectiveness of the proposed capacitor voltage balancing strategy. It shows the voltage waveform for CapYa together with phase A current at secondary side of YY transformer and its switching pulses. The positive direction of the current is defined as flowing out of the converter. It can be seen from the figure at t_1, which is the start of commutation from TY2 to TY4, the capacitor is inserted as a negative voltage to help the commutation. Its voltage decreases as shown in Fig. 14(c) due to

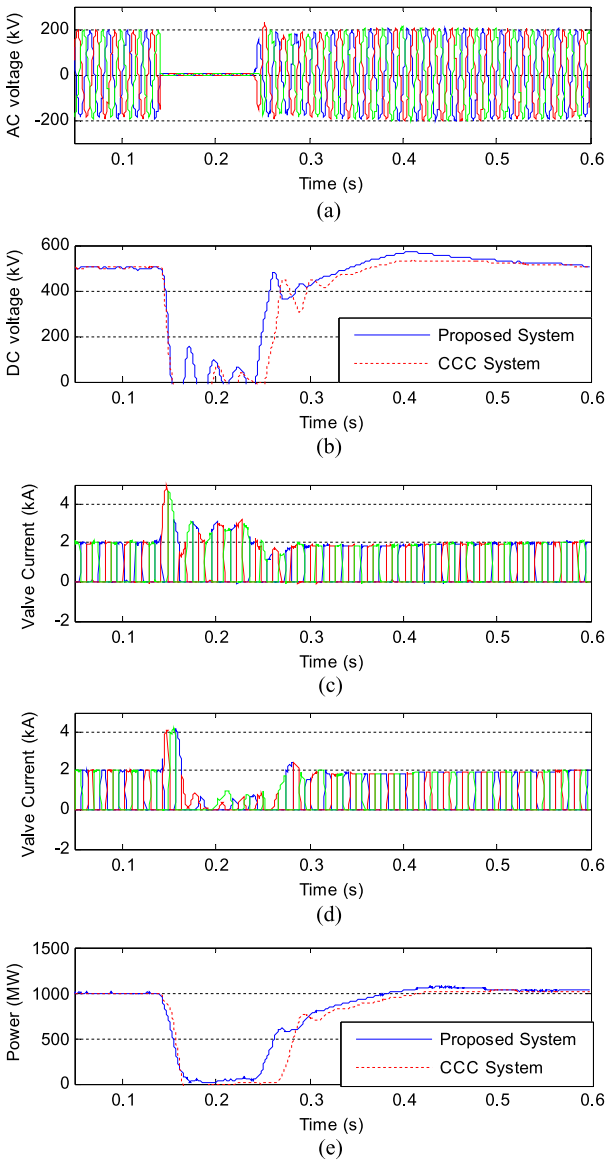

Fig. 13. System response with 100 ms zero impedance three-phase to ground fault at inverter AC bus. (a) AC voltages; (b) Inverter DC voltages; (c) Valve currents (TY2, TY4 and TY6) of the proposed system; (d) Valve currents (TY2, TY4 and TY6) of CCC-HVDC; (e) Power.

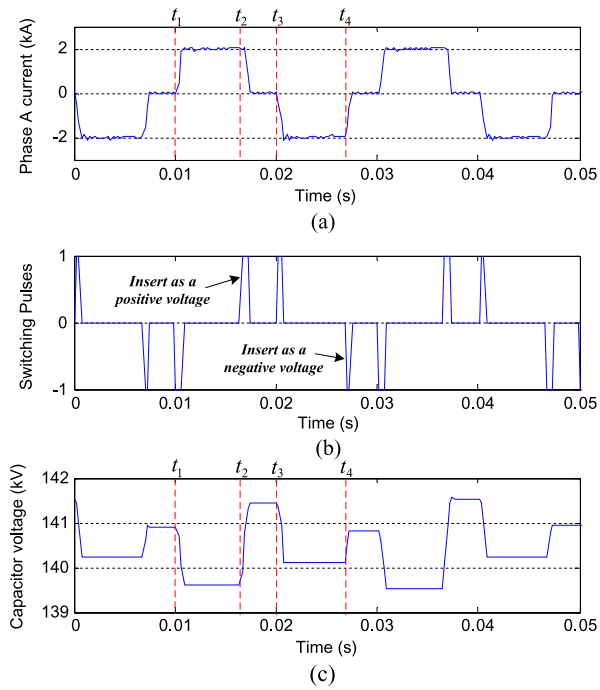

Fig. 14. Capacitor voltage balancing waveforms for CapYa. (a) Phase A current at secondary side of YY transformer; (b) Switching pulses for CapYa; (c) Capacitor voltage of CapYa.

TABLE I
TOTAL HARMONIC DISTORTION COMPARISON

Testing System	AC Voltage THD	AC Current THD
Benchmark System	0.9631%	0.52%
Proposed System	1.12%	0.987%

the direction of the current. At t_2, which is a short period before the start of commutation from TY4 to TY6, the capacitor is inserted as a positive voltage. This is to charge up the capacitor to compensate the net voltage decrease in one cycle. It is not bypassed until commutation is complete. Later in the same switching cycle at t_3 and t_4, the capacitor is inserted in the same ways as described earlier to guarantee the success of commutations. It can also be seen from Fig. 14(b) that the switching frequency of the proposed balancing strategy is 200 Hz.

C. Harmonic Analysis

With the dynamic insertion of capacitors in the commutation loop it is important to examine that the AC voltage and current total harmonic distortions (THD) are not significantly increased. Table I shows the THD comparisons of AC voltage and current between the original benchmark model and the proposed configuration. It can be seen from the table that although both THDs are increased due to the capacitor switching actions, they are still within acceptable limits.

D. Voltage Across Main Thyristors

The valve forward voltage in the proposed system is compared with that of the original CIGRE HVDC benchmark system in Fig. 15. It can be seen from the figure that the voltage stress of the thyristor in the proposed system is comparable to that of the original CIGRE HVDC benchmark system.

VI. LOSS ESTIMATION

In this section, contribution of losses from the series connected capacitor modules are estimated for the proposed system configuration. Both conduction losses and switching losses are calculated using the parameters from manufacture's data sheet. The IGBT module used for calculation is the ABB's HiPak module with maximum collector-emitter voltage of 4.5 kV and maximum DC collector current of 1.2 kA [18]. To be able to safely conduct 2 kA rated DC current, four IGBT modules are connected in parallel and each of them is taking 500 A

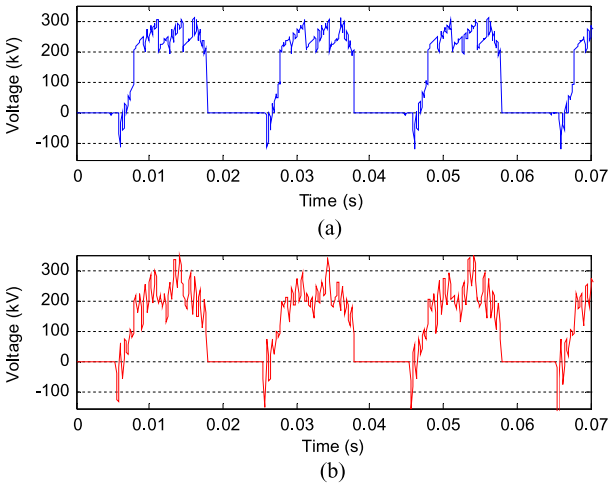

Fig. 15. Voltage stress across the thyristor valves. (a) Original CIGRE HVDC benchmark system; (b) Proposed system.

TABLE II
CONDUCTING DEVICES AND DURATION FOR CAPYA

Commutation (Conduction) Period	Conducting devices	Time duration (deg)
From TY2 to TY4	S2Ya and S3Ya	10
TY3 and TY4 in conduction	S2Ya and D4Ya	110
From TY4 to TY6	D1Ya and D4Ya	10
From TY5 to TY1	S1Ya and S4Ya	10
TY1 and TY6 in conduction	D2Ya and S4Ya	110
From TY1 to TY3	D2Ya and D3Ya	10

at normal condition. 50 of such modules are needed for each phase with nominal collector-emitter voltage of 2.8 kV.

A. Conduction Loss

In order to calculate conduction loss the conduction periods of IGBTs and diodes in capacitor module CapYa over one AC cycle are evaluated as an example. Table II shows the semiconductor devices in conduction and their conduction time for one cycle. The commutation overlap time is reduced to about 10 degrees due to the additional commutation voltage from capacitors. At a given current the voltage drop between the collector and emitter terminals for an IGBT can be calculated as [19]

$$V_{CEtotal} = V_{CEsat}(I_C) + R_{CC'+EE'} I_C \tag{29}$$

where V_{CEsat} is the collector-emitter saturation voltage at specified condition, l_C is the DC collector current and $R_{CC'+EE'}$ is the terminal-to-chip resistance.

Then the conduction loss for this IGBT can be calculated by the integration of forward losses:

$$P_{cond\_IGBT} = \frac{1}{T_0} \int_0^T V_{CEtotal} \times I_C dt \tag{30}$$

where T_0 is the time of one cycle and $\mathbf{T}$ is the conduction time.

The conduction loss of diodes can be calculated in similar ways as that for IGBT except that the diode forward voltage V_F is used instead of collector-emitter voltage. The valve current during commutation period is considered to be linear for simplicity. Once the conduction loss for each IGBT module is obtained, it is scaled to get the total conduction loss for 12-pulse inverter terminal.

TABLE III
SWITCHING LOSS EVALUATION FOR CAPYA

Switching Points	Switching Actions
Completion of commutation from TY2 to TY4	S3Ya turns off
Start of commutation from TY4 to TY6	S2Ya turns off
Completion of commutation from TY5 to TY1	S1Ya turns off
Start of commutation from TY1 to TY3	S4Ya turns off

TABLE IV
LOSS CALCULATION RESULTS FOR THE PROPOSED SYSTEM

	$25\ ^0C$	$125\ ^0C$
Conduction Loss	1.754 MW	1.939 MW
Switching Loss	0.42 MW	0.66 MW
Total Loss	2.174 MW	2.599 MW

B. Switching Loss

To calculate switching losses, the capacitor module CapYa is again considered over one cycle. The switching actions that contribute to switching losses are listed in Table III. For the case of diode, the turn-on energy is neglected. From the table it can be seen that four switching actions over one cycle contribute to switching losses. The total switching loss over the cycle is calculated by reading the turn-off switching energy E_{off} from the data sheet. In similar ways as the calculation of conduction loss, the total switching loss for inverter terminal is obtained by scaling the results for each IGBT module.

Now by using the parameters from data sheet [18], losses can be calculated which are listed in Table IV. The results at two different junction temperatures (25 °C and 125 °C) are presented. Since the series capacitor modules are only connected at the inverter side with rectifier side unchanged, the percentage of loss increase per converter station is between 0.109% to 0.13%. So it can be seen that extra losses from the series connected power electronic devices are not significant.

VII. CONCLUSION

A 'push' & 'pull' method utilizing dynamic capacitor insertion has been proposed to eliminate commutation failures in traditional LCC-HVDC system. The method increases the effective commutation voltage and enables successful commutation even in the absence of AC commutation voltage during fault conditions, i.e. zero impedance three-phase grounding fault. The performance of the method has been tested using the RTDS with small time step simulations. The results have demonstrated that for both zero impedance single-phase and three-phase grounding faults, the commutation failure does not happen. The system is still able to transfer a certain amount

of power during single-phase fault and is able to achieve fast recovery from three-phase fault.

Considering the additional switching devices and capacitors, the proposed hybrid configuration will result in higher cost than the conventional LCC HVDC configuration. However significant improvements in performance are achieved including the elimination of commutation failures.

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